Current Saturation in Few-layer MoS_2 FET

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The discovery of graphene in 2004 has sparked great interest in 2-dimensional (2D) materials for their use in the next generation of electronic devices.[1] Although graphene exhibits some remarkable and really unique electrical properties that may help overcome some of the main limitations in analog electronics,[2][3] its lack of bandgap has limited its use for digital applications. On the other hand, molybdenum disulphide (MoS_2), another two-dimensional material with a band gap of 1.8 eV in single layer and 1.2 eV in bulk, has recently been used in field effect transistors with excellent gate modulation and current pinch-off.[4][5][6] Monolayer MoS_2 is composed of one layer of molybdenum atoms sandwiched between two layers of sulphur atoms for a total thickness of 0.65 Å. Mobility around 300 $cm^2/V.s$ and an on-off current ratio exceeding 10^7 have been experimentally demonstrated while a large g_m (4.4 mS/μm) and excellent short channel behavior (drain induced barrier lowering ~10 mV/V and subthreshold swing ~60 mV/decade with gate length of 15nm) have been predicted. Its potential to reduce short channel effect in highly scaled devices thanks to its excellent electrostatic confinement, together with its high thermal stability, chemical inertness and mechanical properties makes MoS_2 transistors excellent candidates for low power mixed-signal electronics. In this paper, we show MoS_2 FETs with current saturation, for the first time. The saturation behaviour is extremely important for building both digital and analog circuits. This property is lacking in most graphene FETs due to its zero bandgap and is also not observed in the MoS_2 FETs reported in the literature so far.

Few-layer MoS_2 flakes are first obtained from bulk crystals using adhesive-tape-based micromechanical exfoliation onto degenerately-doped Si substrates covered with 285nm thick SiO_2. The sample was then annealed at 300C for 6 hours in forming gas (20 sccm H_2 and 600 s ccm Ar) to flatten the flakes and remove the tape residues. The number of layers in the MoS_2 flake is then confirmed by optical microscopy, Raman spectrum and Atomic Force Microscopy (AFM). The exfoliated MoS2 flakes we investigate always have 1 layer to 6 layers with thickness of 0.7 to 4nm. Figure 1(a) shows the optical micrograph of a typical few-layer MoS_2 flake. The Raman spectrum (Inset of Figure 1 (a)) was measured at room temperature using a 532 nm laser. Two peaks at 384 and 405 cm^{-1} are attributed to the in-plane E^1_{2g} and out-of-plane A_{1g} vibration of MoS_2 respectively.[7] The AFM image (Figure 1(b)) demonstrates that the current sample has very clean and flat surface. This flake contains 5 layers of MoS_2, with a total thickness of 3.5 nm, as shown in the step image in the inset of figure 1(b). The metal contacts are defined using electron beam (e-beam) lithography, followed by deposition of 3 nm titanium / 50 nm gold metal stacks using e-beam evaporation. Figure 1(c) shows an optical micrograph of two parallel FET devices fabricated on the flake in Figure 1(a). They have a gate length of 2 μm and gate width of 3.5 μm.

DC characterization is performed using an Agilent 4155C Semiconductor Parameter Analyzer. All the fabricated few-layer MoS_2 FETs exhibit clear n-type conduction and transistor behaviour (Figure 1(d)), which is consistent with the previous reports. [4][5] The transfer characteristics demonstrate the ability to modulate the resistance of the MoS_2 channel by changing the back-gate voltage, demonstrating an on/off current ratio of about 10^6. The device also shows clear current saturation behavior in its output characteristics (Figure 1(e)). At the lower drain bias region, the current increases almost linearly with V_{DS}. The device is in its linear (triode) region. At higher drain bias, the current changes little with the increase in V_{DS}, showing that the gate voltage can independently change the current. The knee voltages for saturation are 0.1V, 0.2V, 0.5V and 0.6V for Vg=20V, 40V, 60V and 80V, respectively, which is

consistent with theoretical work. [6] The output conductance ($gd=\partial I_D/\partial V_{DS}$) is 4.3, 2.8, 1.2 μS/μm for V_g=80, 60, 40V, respectively. Such saturation is observed in many of our devices. Figure 1(f) shows the output characteristics of a second MoS_2 FET fabricated using photolithography. It has a channel length of 1.6 μm, width of 24 μm and thickness of 2.1 nm. At V_g=40V, the saturation current is 160 μA, corresponding to a current density of 6.7 μA/μm. The output conductance is 6.1, 4.6, 3.0, 1.1 μS/μm for V_g=40, 20, 0, -20V, respectively. In the lower bias region, the device shows some Schottky response and the current rise a little with the increase of drain and source voltage in the saturation region. It is believed that the Schottky behaviour may be due to photoresist residue in the contact region.

In conclusion, we have fabricated few-layer MoS_2 FETs and characterized their electronic performance. These devices show on/off current ratios larger than 10^6, current density as large as 6.7 μA/μm. In addition, current saturation has been observed for the first time in MoS_2 FETs, which is extremely important for building both digital and analog circuits.

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Figures

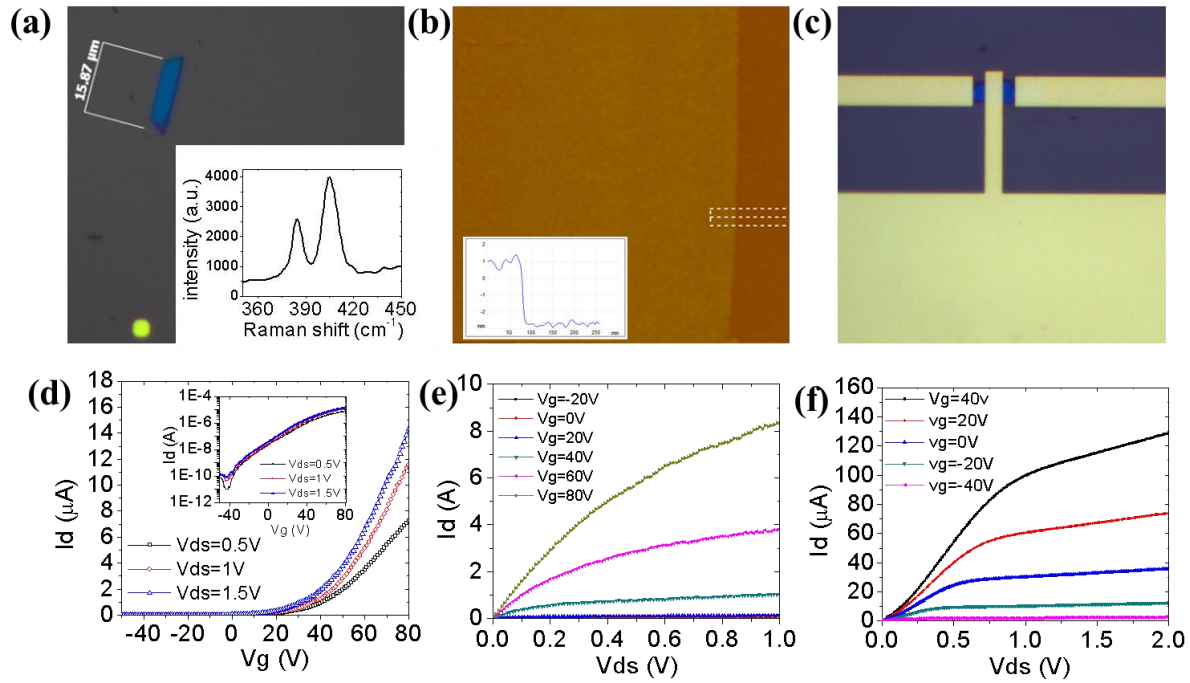

Figure1. ***(a)*** *Optical micrograph, Raman spectra (inset) and* ***(b)*** *AFM image of few-layer MoS_2 flake.* ***(c)*** *Optical image of two parallel MoS_2 field-effect transistors fabricated by electron-beam lithography.* ***(d)****Room temperature transfer characteristic for the FET in c). The inset shows the transfer characteristic in logarithmic scale to demonstrate the on/off current ratio of >10^6.* ***(e)*** *Output characteristics of the FET in (c) with back gate voltage from -20V to 80 V in steps of 20V.* ***(f)*** *Output characteristics of another FET fabricated by photolithography with back gate voltage from -40V to 40 V in steps of 20 V.*